Second-Generation Power Supply Interface (PSI_II) Manual

April 4, 2007

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Overview

There are hundreds of power supplies in Brookhaven National Laboratory's (BNL) Booster, AGS and RHIC. The power supplies control magnets and other equipment. The control interface for each power supply should meet the following criteria:

1. Provide a "standard" interface to power supply vendors through a uniform electrical/mechanical interface.
2. Provide isolation between the control system and the power supply.

Based on these requirements, a second-generation power supply interface called PSI_II (to differentiate from the previous PSI units) has been designed. The PSI_II is a 1U, 19-inch rack mounted unit, with standardized power supply analog and digital interfaces. The communication link between the controller (V233) and a PSI_II is through fiber optic cables, which provide both isolation and extensibility.

A power supply is usually controlled with an analog reference voltage, called a setpoint, and digital signals, called commands. A power supply's ramping function consists of a series of sequential setpoints. Typical power supply commands are ON, OFF, STANDBY, and RESET.

The operational state of a power supply is usually monitored through its analog output voltages and digital status signals, called readbacks. A readback voltage can represent the power supply's current measured by a shunt or DC current transformer (DCCT), or it can represent the magnet and cable's voltage drop. Status signals convey the power supply's run state and any fault conditions. Normally, each setpoint sent from the V233 to a power supply via a PSI_II results in six readbacks: a setpoint echo, a digital status word, and four analog values. Each word sent between a V233 and a PSI_II incorporates a checksum to help ensure error free transmissions.

Many power supplies need to be ramped rapidly with a fine resolution. The V233 – PSI_II combination communicates over fiber optic links operating at 50Mbs. This allows setpoints to be sent at a maximum rate of 100,000 per second. The fiber optic links utilize a bi-phase mark encoded data stream. Unlike the original PSI, a data and clock recovery chip is utilized to synchronize to the data stream and decode the information.

The PSI_II's gate array design was created using the Verilog hardware design language and Xilinx's latest design software. Simulation was done using Mentor Graphics' ModelSim software. Both the design and the simulation are easy to maintain and to upgrade. They can also be ported into a different design environment.

System Description

Figure 1 is a block diagram showing a typical power supply control system.

The FEC loads a function into the V233 via the VME bus. The V233 stores the digitally represented setpoints in its buffers. When triggered by a timing signal from an event link, the V233 commences sending setpoint to the PSI_II at a maximum rate of 100,000 setpoints per second. Upon receiving each setpoint, the PSI_II's DAC (digital to analog converter) converts the setpoint to an analog output. At the same time, four ADCs (analog to digital converter) on the PSI_II take samples of the four analog voltage inputs, and converts them to digitally represented readbacks. These analog readbacks, as well as the digital status readback and echo readback, are immediately sent back to the V233, which saves them in buffers. This setpoint/readback cycle takes less than 10 microseconds.

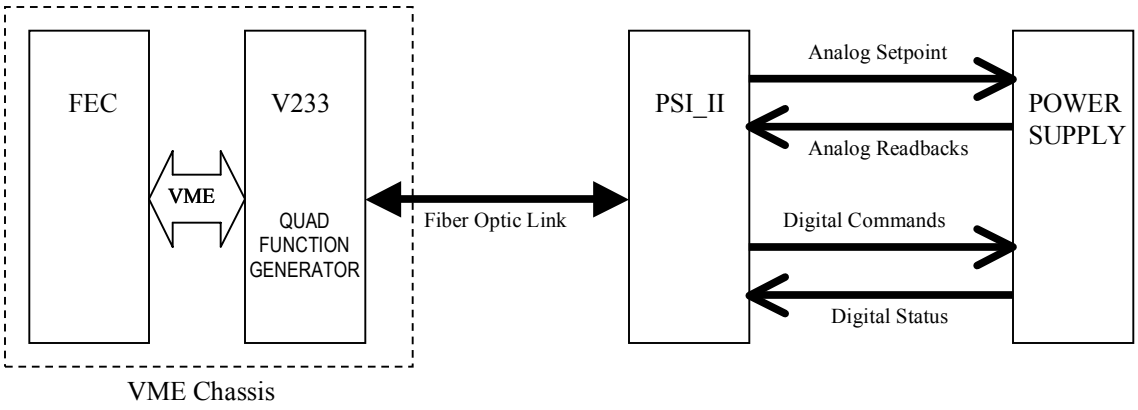

Figure 1. Power supply control system with a V233 and a PSI_II

In a similar manner, individual digital commands can be sent from the V233 to the PSI_II. After receiving the command, the PSI_II sets the appropriate power supply command bits, and responds to the V233 with an echo and the power supply's status.

Figure 2 shows the block diagram of a PSI_II. It consists of four major sections: The V233 interface, the power supply interface, the FPGA block, and the power module. The ensuing paragraphs give details of each section.

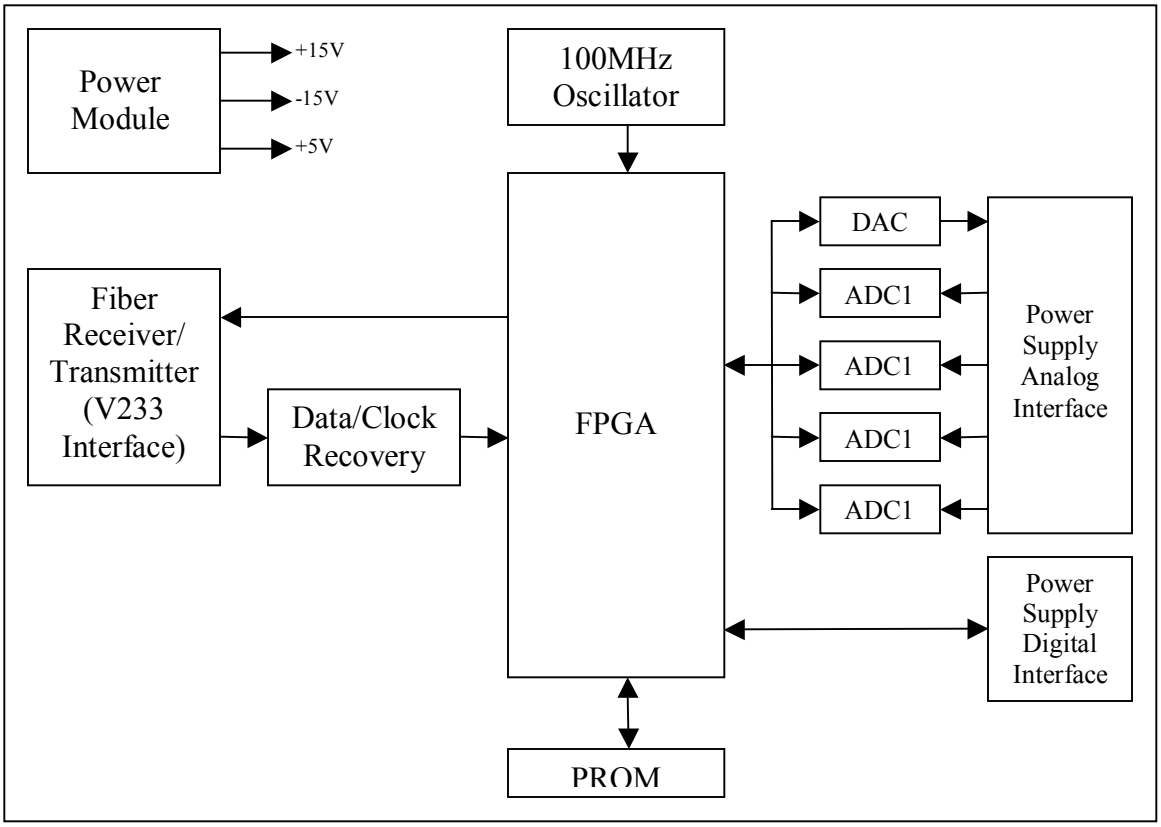

Figure 2. PSI_II Block Diagram

1.0) V233 Interface

1.1) Fiber Optic Link

There are two fiber optic connections between a V233 and a PSI_II; one for the V233 to transmit setpoints and commands to the PSI_II, and one for the V233 to receive readbacks and status from the PSI_II. The data is formatted using a self-clocking bi-phase mark encoding scheme, resulting in a data stream running at 50Mbs. This is shown in Figure 3. The carrier is continuous. During idle periods, when no data is being sent, only "ones" are transmitted.

A low voltage fiber optic transceiver (1300nm wavelength, 62.5/125 or 50/125 multimode fiber) is used to communicate with a V233. The transceiver is packaged in an industry standard 1x9 SIP package, with a duplex ST connector interface, and is powered by 3.3Vdc.

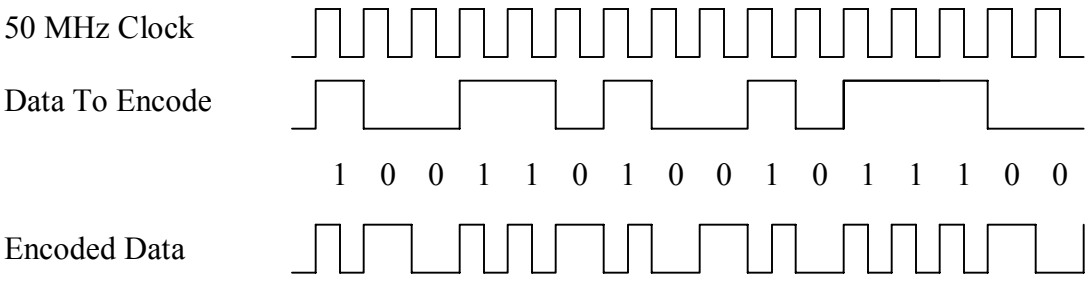

Figure 3. Biphase Mark Encoding

1.2) Bi-phase Mark Encoder and Decoder Circuit

The encoding and decoding functions are performed in the same XILINX FPGA chip. The encoder circuit provides a bi-phase mark format. Bi-phase mark has two advantages over standard NRZL data transmission. First, there is always at least one level transition every bit period. This feature makes it easier to synchronize to the signal for decoding purposes. Second, it allows for more stable transmitting power.

To reliably decode a 50Mbs bi-phase mark data stream, a data and clock recovery (DCR) chip is used. The DCR chip is designed to synchronize to an NRZL data stream operating between 32Mbs and 175Mbs. It accepts a differential PECL input signal, and the data and clock outputs are single-ended PECL signals. It also provides a TTL link fault indication.

1.3) Frame Encoder

Data words sent between a V233 and the PSI_II (setpoints, readbacks, commands and statuses) are all formatted into a structure called a frame. A frame consists of 43 bits, as shown below in Figure 4.

Start (1)	ID (8)	Data (16)	Auxiliary (8)	CRC (8)	Stop (2)

1 Start Bit	Always “0”
8 Frame ID Bits	Frame ID identifies data type (setpoint, command, etc.)
16 Data Bits	Normally formatted in two’s complement
8 Auxiliary Bits	Only active in setpoints
8 CRC Bits	Error checking polynomial = $x^8+x^7+x^5+x^4+x+1$, excluding start and stop bits
2 Stop Bits	Always “11”

Figure 4. Frame Structure

1.4) Data Exchange Protocols

To minimize high-level software incompatibility, the data exchange protocols between a V233 and a PSI_II are similar to the protocols used in the original PSC-PSI system. Table 1 shows the different protocols.

Protocol	V233 Frame	Delay	PSI_II Response					
			Frame 1	Frame 2	Frame 3	Frame 4	Frame 5	Frame 6
Set setpoint Read status & readbacks	ID=0x15 Data=Setpoint Aux.= Aux. Bits	1.5us	Same as Received Frame	ID=0x93 Data=Status Aux.= 0x0	ID=0x80 Data=ADC1 Aux.= 0x0	ID=0x90 Data=ADC2 Aux.= 0x0	ID=0xA0 Data=ADC3 Aux.= 0x0	ID=0xB0 Data=ADC4 Aux.= 0x0
Send command. Read status & readbacks	ID=0x0A Data=Command Aux.=Not used	1.5us	Same as Received Frame	ID=0x93 Data=Status Aux.= 0x0	ID=0x80 Data=ADC1 Aux.= 0x0	ID=0x90 Data=ADC2 Aux.= 0x0	ID=0xA0 Data=ADC3 Aux.= 0x0	ID=0xB0 Data=ADC4 Aux.= 0x0
Read status & readbacks	ID=0x40 Data=Not used Aux.=Not used	1.5us	Same as Received Frame	ID=0x93 Data=Status Aux.= 0x0	ID=0x80 Data=ADC1 Aux.= 0x0	ID=0x90 Data=ADC2 Aux.= 0x0	ID=0xA0 Data=ADC3 Aux.= 0x0	ID=0xB0 Data=ADC4 Aux.= 0x0
Set setpoint only	ID=0x55 Data=Setpoint Aux. = Aux Bits	3us	Same as Received Frame					
Send command only	ID=0x4A Data=Setpoint Aux.= Not used	0us	Same as Received Frame					
Read setpoint & command	ID=0x00 Data=Not used Aux.=Not used	0us	Same as Received Frame	ID=0x95 Data=Command Aux.= 0x0	ID=0x8A Data=Setpoint Aux.= 0x0			
Read Configuration	ID=0x01 Data=Not used Aux.=Not used	0us	Same as Received Frame	ID=0x96 Data={version, configuration switch (S1) setting} Aux.= 0x0	ID=0x8B Data={11'b0, fiber_good, ADC_busy[3:0]} Aux.= 0x0			
ADC Auto Calibration (calibration takes 1.2 second to finish)	ID=0x02 Data= Not Used Aux.= Not used	3us	Same as Received Frame					

Table 1. Data Exchange Protocols

All communications between the V233 and the PSI_II are initiated by the V233. There are eight different communication protocols:

1.4.1) Set setpoint and read status plus four analog values (FrameID=0x15)

The V233 initiates the cycle by sending a setpoint to the PSI_II. Upon receiving this frame, the PSI_II starts a DAC operation. Once the DAC is done, the four ADC chips take samples from the four analog inputs, and start A-to-D conversions. Six frames will be sent back to the V233: echo (a copy of the received frame), status, ADC1, ADC2, ADC3 and ADC4. The entire communication cycle (from the beginning of the V233 setpoint frame to the end of the PSI_II's response frame) take less than 10us. This means that the V233 can send setpoints to the PSI_II at a maximum rate of 100,000 setpoints per second.

There is one difference between a V233/PSI_II setpoint cycle and a slower PSC_PSI setpoint cycle. In a PSC_PSI system, setpoints are sent at a maximum rate of 10,000 setpoints per second. There is enough time (100 microsecond) for both the DAC and

ADCs to finish their conversions within the same cycle. In the faster V233_PSI_II cycle, it is impossible for both the DAC and ADCs to finish their conversions in the same 10us cycle. The PSI_II finishes the DAC conversion, starts the ADC conversions, and returns the ADC results from the previous cycle. In another word, there is one cycle delay for the four readbacks.

1.4.2) Send command and read status plus four analog values (FrameID=0x0A)

The V233 sends a command frame to control the digital outputs. Once the PSI_II receives this frame, it drives the command data onto the digital output connector. Then the PSI_II sends back six frames: echo, status, ADC1, ADC2, ADC3 and ADC4. The four ADCs are the results from the previous ADC conversion cycle. A new ADC conversion is initiated, and the results are saved for the next cycle.

1.4.3) Read status plus four analog values (FrameID=0x40)

The V233 sends a frame with FrameID=0x40 to acquire the digital status and the analog readbacks. The PSI_II sends back six frames: echo, status, ADC1, ADC2, ADC3 and ADC4. The four ADCs are the results from the previous ADC conversion cycle. A new ADC conversion is initiated, and the results are saved for the next cycle.

1.4.4) Set setpoint only (FrameID=0x55)

The V233 sends a setpoint to the PSI_II. The PSI_II finishes the DAC conversion, and sends an echo frame back to the V233. This command is used in applications where status and analog readbacks are not required.

1.4.5) Send command only (FrameID=0x4A)

The V233 sends a command to the PSI_II. The PSI_II simply drives the command data onto the digital output connector, and returns an echo frame back to the V233.

1.4.6) Setpoint and command readback (FrameID=0x00)

This communication cycle is designed for the V233 to retrieve the current (last) setpoint and command from the PSI_II. The PSI_II responds by sending backs three frames: echo, setpoint, and command.

1.4.7) Read configuration (FrameID=0x01)

This communication cycle is designed for the V233 to retrieve the PSI_II's version, configuration, and status. The PSI_II responds by sending backs three frames: echo, PSI version/configuration, and PSI status.

PSI Version/Configuration Data

Bits 15:8	Firmware Version
Bit 7	Bipolar/Unipolar Mode; 1 = Bipolar, 0 = Unipolar
Bit 6	Command Mode; 1 = Command Pulse Mode, 0 = Command Static Mode This refers to the four command bits, ON, OFF, STANDBY, and RESET. In pulse mode, these bits are pulsed to their active state for 100ms, and return to their inactive state. In static mode, these bits are set to their active state and remain there.

Bit 5	Command Polarity; 1 = Active Negative, 0 = Active Positive
Bit 4	Digital Output 1- 4 Mode; 1 = Pulse Mode, 0 = Static Mode This refers to bits 5 through 8 of the Command word. In pulse mode, these bits are pulsed to their active state for 100ms, and return to their inactive state. In static mode, these bits are set to their active state and remain there.
Bit 3	Digital Output 1- 4 Polarity; 1 = Active Negative, 0 = Active Positive
Bit 2	Digital Output 5- 7 Mode; 1 = Pulse Mode, 0 = Static Mode This refers to bits 9 through 11 of the Command word. In pulse mode, these bits are pulsed to their active state for 100ms, and return to their inactive state. In static mode, these bits are set to their active state and remain there.
Bit 1	Digital Output 5- 7 Polarity; 1 = Active Negative, 0 = Active Positive
Bit 0	Test/Normal Mode; 1 = Test Mode, 0 = Normal Mode

PSI Status Data

Bits 15:5	Not Used
Bit 4	Fiber Input Good
Bit 3	ADC 4 Busy
Bit 2	ADC 3 Busy
Bit 1	ADC 2 Busy
Bit 0	ADC 1 Busy

1.4.8) ADC Auto Calibration (FrameID=0x02)

The V233 uses this communication cycle to send an auto calibration command to the PSI_II. The calibration will take 1.2 second to finish. During the auto calibration period, the four ADC chips will be busy and cannot perform any conversions.

2.0) Power Supply Interface

The digital and analog power supply interface of the PSI_II is similar to that of the PSI in order to provide a seamless transfer from one to the other. The analog signals are carried in and out of the PSI_II through a 9-pin D-Sub connector.

2.1) Analog Interface

Table 2 below shows the pin assignments of the 9-pin analog connector. There is one setpoint voltage output, and four readback voltages. The names given to the analog inputs are common for many power supplies used in the accelerator complex.

The DAC and ADC chips used in a PSI_II are the same as that used in PSI.

PIN	FUNCTION
1	ANALOG INPUT4: CURRENT ERROR
2	ANALOG INPUT3: MEASURED VOLTAGE
3	ANALOG INPUT2: MEASURED CURRENT
4	ANALOG INPUT1: CURRENT SETPOINT
5	ANALOG OUTPUT: SETPOINT
6	INPUT SHIELD
7	INPUT RETURN
8	SETPOINT SHIELD
9	SETPOINT RETURN

Table 2. Pin Assignments For 9-pin D-Sub Analog Connector

2.2) Digital To Analog (DAC) Conversion

The PSI_II uses an Analog Device AD669 as the on-board DAC to supply the power supply reference voltage. It is a complete 16 bit monolithic DAC, equipped with an output amplifier that can be configured as a unipolar (0Vdc to +10Vdc) or bipolar (-10Vdc to +10Vdc) output. Switch S1 of the PSI_II selects the output range.

The AD669 will provide a minimum of 5mA of current at the output. Its architecture insures 15-bit monotonicity over temperature, and internal nonlinearity is maintained at +/- 0.003%, while differential nonlinearity is +/- 0.003% maximum. The output amplifier provides a voltage output settling time of 10 microseconds, to within 2 LSBs for a full-scale step.

One improvement of the PSI_II over the PSI can be seen during power-up. When a PSI is first powered, there is a voltage spike at the DAC output. This is a characteristic of the AD699 during initialization. Clearly, this voltage spike is not desirable, especially when connected to an operating power supply. To overcome this problem in the PSI_II, a reed relay is used to temperately short the DAC output, so the spike is suppressed during power-up. This solution is based on one important feature of AD699: its output can be indefinitely shorted to ground, with a typical short circuit current of 25mA.

2.3) Analog To Digital (ADC) Conversion

Analog Device's ADC677 is an excellent fit for the PSI and PSI_II, since it includes an auto calibration function that provides excellent DC performance, and eliminates the need for user adjustments.

Typical specs over temperature include:

Resolution and Differential Nonlinearity (No missing codes): 16 bits
Integral Nonlinearity: +/-1 LSB
Bipolar Zero Error: +/-1 LSB
Positive/Negative Full Scale Errors: +/- 1 LSB
Temperature Drift: +/- 0.5 LSB

Performance can also affected by the reference voltage supplied to the ADC. The reference source selected (AD587) has a maximum deviation of +/- 3.5 mV between 0 and 70 degrees C, or a maximum temperature coefficient of 5ppm/^{o}C. Sourcing 10.000 V to the ADC, an input bipolar voltage of +/- 10V is converted to 16 bits.

To isolate the power supply measurement source from the ADC's dynamic input characteristics during conversion, a precise, high slew rate, low drift amplifier (Analog Devices' AD845) precedes each ADC. The AD587 has not only low drift and high precision, but also a high slew rate (100V/us) that can easily follow a rapidly ramping signal.

2.4) Digital Interface

The digital interface between a PSI_II and a power supply is based on standard TTL logic. The digital signals are carried in and out of the PSI_II through a 37-pin D-Sub connector. The pin assignments are shown in Table 3. Many of the names shown in the Function column, especially the statuses, are derived from typical applications, but are not limited to those specific purposes.

Most of the digital input and output signals are the same for the PSI and the PSI_II. However, there are two additional features in the digital outputs of a PSI_II.

2.4.1) Fused +5V, 1A Output

As shown in Table 3, there is a fused +5V output on pin 7 of the 37-pin D-Sub connector. The output is routed through a 1A on-board fuse. This +5V DC supply is provided for any hardware applications that may require it.

2.4.2) Auxiliary Bits

As shown in Table 3, there are three auxiliary output bits. These auxiliary bits are not controlled as part of a command. Instead, they are controlled through the auxiliary bits of a setpoint frame. This design is for applications where digital output bits need to be sent along with a setpoint.

PIN	FUNCTION	Control/Readback bit
1	ON (COMMAND OUTPUT)	Command bit [0] output.
2	STANDBY (COMMAND OUTPUT)	Command bit [2] output.
3	NEG. POLARITY (COMMAND OUTPUT)	Command bit [4] output.
4	DIGITAL OUT # 2 (COMMAND OUTPUT)	Command bit [6] output.
5	DIGITAL OUT # 4 (COMMAND OUTPUT)	Command bit [8] output.
6	DIGITAL OUT # 6 (COMMAND OUTPUT)	Command bit [10] output.
7	FUSED +5V OUTPUT	Fused +5V output.
8	AUXILIARY BIT 1	Aux. Bit [1] output. Set by setpoint command.
9	SIGNAL GND	GND.
10	SIGNAL GND	GND.
11	SIGNAL GND	GND.
12	OFF (STATUS INPUT)	Status input bit [1].
13	NEGATIVE (STATUS INPUT)	Status input bit [3].
14	OVERVOLTAGE (STATUS INPUT)	Status input bit [5].
15	OUT OF REG. (STATUS INPUT)	Status input bit [7].
16	OVER TEMP. (STATUS INPUT)	Status input bit [9].
17	WATER MAT (STATUS INPUT)	Status input bit [11].
18	GND FAULT (STATUS INPUT)	Status input bit [13].
19	PHASE FAULT (STATUS INPUT)	Status input bit [15].
20	OFF (COMMAND OUTPUT)	Command bit [1] output.
21	RESET (COMMAND OUTPUT)	Command bit [3] output.
22	DIGITAL OUT # 1	Command bit [5] output.
23	DIGITAL OUT # 3	Command bit [7] output.
24	DIGITAL OUT # 5	Command bit [9] output.
25	DIGITAL OUT # 7	Command bit [11] output.
26	AUXILIARY BIT 0	Aux. Bit [0] output. Set by setpoint command.
27	AUXILIARY BIT 2	Aux. Bit [2] output. Set by setpoint command.
28	SIGNAL GND	GND.
29	SIGNAL GND	GND.
30	ON (STATUS INPUT)	Status input bit [0].
31	STANDBY (STATUS INPUT)	Status input bit [2].
32	FAULT SUMMARY (STATUS INPUT)	Status input bit [4].
33	OVER CURRENT (STATUS INPUT)	Status input bit [6].
34	FAN FAULT (STATUS INPUT)	Status input bit [8].
35	WATER FLOW (STATUS INPUT)	Status input bit [10].
36	SECURITY (STATUS INPUT)	Status input bit [12].
37	RIPPLE FAULT (STATUS INPUT)	Status input bit [14].

Table 3. Pin Assignments For 37-pin D-Sub Digital Connector

3.0) FPGA Block

3.1 Field-Programmable Gate Array (FPGA)

The Xilinx Spartan-3 (XC3S400) field-programmable gate array (FPGA) is used to control the logic of the PSI_II. The XC3S400 has 400,000 system gates, and 344,000 bits of embedded memory. A precise 100MHz oscillator with frequency stability of 50ppm (CTS CB3LV-100) is used for clocking the XC3S400.

An in-system configuration PROM (Xilinx XCF08) is used to program the FPGA upon power-up. The FPGA program was developed in Verilog Hardware Design Language, using Xilinx's ISE platform. All simulations were performed with Mentor Graphics's ModelSim simulation software.

3.2 Switch S1

Although the FPGA program file is stored in PROM and cannot be changed, there is an on-board switch (S1) that allows some of the PSI_II's operating parameters to be selected by the user. Table 4 shows the functions of the switch.

S1 Pin	Function	Details
1	Power supply polarity: Unipolar vs. Bipolar	ON: To control a unipolar power supply (combined with DAC jumper setting J5) OFF: To control a bipolar power supply (combined with DAC jumper setting J5)
2	On/Off/Stby/Reset: Static vs. Pulse	ON: ON/OFF/StandBy/Rest command bits are static signals OFF: ON/OFF/StandBy/Rest command bits are pulse signals
3	NEG_POL: Static vs. Pulse	ON: NEG_POL command bit is a static signal OFF: NEG_POL command bit is a pulse signal
4	Digital_Out[1:4]: Static vs. Pulse	ON: Digital_out[1:4] are static signals OFF: Digital_out[1:4] are pulse signals
5	Digital_Out[1:4] Polarity: Positive vs. Negative	ON: Digital_out[1:4] have positive polarities OFF: Digital_out[1:4] have negative polarities
6	Digital_Out[5:7]: Static vs. Pulse	ON: Digital_out[5:7] are static signals OFF: Digital_out[5:7] are pulse signals
7	Digital_Out[5:7] Polarity: Positive vs. Negative	ON: Digital_out[5:7] have positive polarities OFF: Digital_out[5:7] have negative polarities
8	Mode: Normal vs. Test mode	ON: PSI_II is in normal mode OFF: PSI_II is in test mode

Table 4. Functions Controlled By On-Board Switch S1

All switch settings should be made prior to applying power to the PSI_II.

There are four main parameters that are controlled with switch S1.

3.2.1) Output Range Of Analog Reference Voltage

The PSI_II can be configured to generate a unipolar or bipolar analog voltage reference. This is controlled by rocker1 of S1, in concert with Jumper J5. J5 directly sets the DAC to either unipolar or bipolar mode. Rocker1 of S1 makes sure that the FPGA presents data to the DAC in the required format. The DAC will output 0Vdc to 10Vdc in unipolar mode, and –10Vdc to +10Vdc in bipolar mode.

3.2.2) Static Or Pulse Mode

Some power supplies only accept pulsed command signals and pulsed digital outputs. S1 controls different sets of output bits (see Table 4) to operate in static or pulse mode. When pulse mode is selected, the pulse width is fixed at 100ms.

3.2.3) Command Or Digital Signal Polarity

Some power supplies require negative polarity command bits or digital output bits. S1 controls different sets of output bits (see Table 4) to operate with positive or negative polarity.

3.2.4) Normal Mode Or Test Mode

To carry out a simple operational check on a PSI_II without a V233 or any external test software, a self-test mode has been incorporated into the design. The self-test mode provides a quick and simple in-field diagnostic of a PSI_II. To put the PSI_II in self-test mode, set rocker8 of S1 to the off position, and configure the PSI_II to operate in bipolar mode. Connect a fiber optic cable directly from the transceiver's TX port to its RX port. After initial power-up, wait 12 seconds for the reset to complete, and then the PSI_II will automatically start to send continuous setpoints to itself. Using a scope, the user should be able to measure a triangle waveform at the DAC output. The waveform should have 8.4ms period, and -10V/+10V peak-to-peak amplitude. In addition, the front panel LEDs (TX, RX, and Set) should be blinking at such a rapid rate that they appear to be constantly on. If an error occurs at any time, such as a CRC error or a FrameID error, the self-test operation will be terminated, and the front panel LEDs will go out. If power is recycled, the self-test will start again. A successful self-test operation will tell the user that the PSI_II's major functions (fiber links, encoder, decoder, FPGA and DAC) are operating correctly.

To return to normal PSI_II operation, power must be turned off and rocker8 of S1 must be set back to normal mode.

4.0) Power Module

4.1) The PSI_II's internal power supply module is made by Phihong, part number PSA4534. It provides three voltages: +15Vdc, -15Vdc, and +5Vdc. The power module's input voltage is 90-264VAC. It generates up to 4A at +5Vdc, 1.2A at +15Vdc and 0.5A at –15Vdc. On the PSI_II's circuit board, a triple-supply power management IC (TI part TPS75003) converts the +5Vdc to the three lower voltages: +3.3Vdc, +2.5Vdc, and +1.2Vdc. These voltages are used by the XILINX FPGA and other peripheral devices.

PSI_II Adaptations

As described in earlier sections of this document, the PSI_II is designed to operate at a maximum rate of 100,000 setpoints per second. It has one reference voltage output, and four analog readbacks. However, during the development of the PSI_II, there have been applications requiring modifications to the basic PSI_II design. These are described below.

Euro-Card PSI_II

In areas requiring many PSIs, there have sometimes been installation space constraints. To help alleviate this problem, another version of the PSI_II has been developed in the form of a Euro-card, assembled with a front panel. The voltages required to operate the PSI_II (+15Vdc, -15Vdc, and +5Vdc), are delivered through the backplane mating connectors P1 and P2, as are the grounds, analog signals, and digital signals. Assembled as Euro-cards, as many 16 or more PSI_II modules can be inserted in a Euro chassis. There is an added benefit of lower cost, since each module is not assembled in its own chassis. One drawback, of course, is that the modules cannot be located immediately next to their associated power supplies. Another potential drawback is that the grounds are tied together. The isolation between power supplies is lost.

A slightly customized VME chassis may be used to house Euro-card PSI_IIs. The standard +12Vdc/-12Vdc VME power supply needs to be replaced with a +15Vdc/-15Vdc power supply. The disadvantage is that other VME modules requiring +12Vdc/- cannot be installed into the same chassis as the PSI_II.

It is possible to power a Euro-card PSI_II through the P2 connector instead of the P1 connector. This allows the use of a standard VME backplane, with +12Vdc/-12Vdc on P1. The user would need to provide +15Vdc/-15Vdc to the PSI_II on the P2 connector. However, other VME modules could then use the same chassis.

Table 5 shows the PSI_II pin assignments for both the P1 and P2 connector. All PSI_II analog and digital signals are all located on P2 connector. Many of the names shown for the status inputs are derived from typical applications, but are not limited to those specific purposes. Aside from the option to power the PSI_II through P1, the PSI_II pin assignments are VME compatible.

PIN/ROW	P1A	P1B	P1C	P2A	P2B	P2C
1	N/C	N/C	N/C	DAC_Vout	+5V(IN)	AGND
2	N/C	N/C	N/C	AGND	DGND	NEGTIVE_A_B_C_D
3	N/C	N/C	N/C	AGND	N/C	POS IN – D
4	N/C	N/C	N/C	AGND	N/C	POS IN – C
5	N/C	N/C	N/C	AGND	N/C	POS IN – B
6	N/C	N/C	N/C	AGND	N/C	POS IN – A
7	N/C	N/C	N/C	N/C	N/C	N/C
8	N/C	N/C	N/C	N/C	N/C	N/C
9	DGND	N/C	DGND	N/C	N/C	N/C
10	N/C	N/C	N/C	N/C	N/C	N/C
11	DGND	N/C	N/C	DGND	N/C	DGND
12	N/C	N/C	N/C	DGND	DGND	+15V(IN)
13	N/C	N/C	N/C	DGND	+5V(IN)	+15V(IN)
14	N/C	N/C	N/C	OFF (OUT)	N/C	PHASE FAULT (IN)
15	DGND	N/C	N/C	RESET (OUT)	N/C	-15V(IN)
16	N/C	N/C	N/C	DIGITAL_OUT1(OUT)	N/C	-15V(IN)
17	DGND	N/C	N/C	DIGITAL_OUT3(OUT)	N/C	ON (OUT)
18	N/C	N/C	N/C	DIGITAL_OUT5(OUT)	N/C	STANDBY (OUT)
19	DGND	N/C	N/C	DIGITAL_OUT7(OUT)	N/C	NEG_POLARITY (OUT)
20	N/C	DGND	N/C	AUX_BIT0(OUT)	N/C	DIGITAL_OUT2(OUT)
21	N/C	N/C	N/C	AUX_BIT2(OUT)	N/C	DIGITAL_OUT4(OUT)
22	N/C	N/C	N/C	DGND	DGND	DIGITAL_OUT6(OUT)
23	N/C	DGND	N/C	DGND	N/C	FUSED_+5V (OUT)
24	N/C	N/C	N/C	ON (IN)	N/C	AUX_BIT1(OUT)
25	N/C	N/C	N/C	STANDBY (IN)	N/C	OFF (IN)
26	N/C	N/C	N/C	FAULT SUMARY (IN)	N/C	NEGTIVE (IN)
27	N/C	N/C	N/C	OVER CURRENT (IN)	N/C	OVERVOLTAGE (IN)
28	N/C	N/C	N/C	FAN FAULT (IN)	N/C	OUT OF REG. (IN)
29	N/C	N/C	N/C	WATER FLOW (IN)	N/C	OVER TEMP. (IN)
30	N/C	N/C	N/C	SECURITY (IN)	N/C	WATER MAT (IN)
31	-15V(IN)	N/C	+15V(IN)	RIPPLE FAULT (IN)	DGND	GROUND FAULT (IN)
32	+5V(IN)	+5V(IN)	+5V(IN)	N/C	N/C	N/C

Table 5. P1 And P2 Pin Assignments

10KHz PSI II

The original PSI was designed to interface with Apogee Lab's PSC. Later, the V133 was developed to work with the same PSI. The fiber optic link for this system operates at 5Mbs, limiting the setpoint transfer rate to a maximum of 10,000 per second. Because it is still desirable to be able to support the PSC and the V133, another version of the PSI_II has been built that uses a fiber optic link rate of 5Mbs.

The data and clock recovery (DCR) chip used in the standard PSI_II does not work in this configuration, since its lowest operating rate is 32Mbs. For the slower fiber optic link rate, a PECL to TTL converter directly converts the link data to TTL, and the FPGA chip itself is used to recover the data and clock. This requires the 10KHz PSI_II to use different FPGA firmware. In addition, the DCR chip is removed from the circuit board. The PECL signals from fiber transceiver are fed directly to the PECL to TTL converter.

Because the 10KHz PSI_II doesn't transfer setpoints and readbacks at the higher rate of the standard PSI_II, the ADCs are able to finish their conversions and report the results in the same cycle.

If necessary, the 10KHz PSI_II can also be manufactured in the Euro-card format discussed earlier.

Dual Output PSI (Push-Pull PSI)

In some instances, particularly in EBIS, there are pairs of power supplies operating in push-pull configurations. While one supply is receiving a positive reference voltage, the other power supply is receiving a negative reference voltage. The voltages have identical amplitudes, but opposite polarity. Two separate PSI_IIs could be used to control the power supply pair, but in the interest of being more space and cost efficient, a dual output PSI_II has been developed.

The dual output PSI_II has two individual DACs. However, setpoints are only sent to the PSI_II for one DAC. The FPGA calculates the opposite polarity setpoint for the other DAC. There are still four ADCs in the dual output PSI_II, which allows two readbacks from each power supply.

In the dual output PSI_II, the 9-pin D-Sub connector is replaced by a 15-pin D-Sub connector. Table 6 shows the pin assignments of the 15-pin analog connector

The digital I/O of the dual output PSI_II is unchanged. The command bits, digital output bits, and status bits must be shared between the two push-pull power supplies.

PIN	FUNCTION
1	NO CONNECTION
2	NO CONNECTION
3	ANALOG OUTPUT2: SETPOINT 2
4	ANALOG INPUT4: CURRENT ERROR
5	ANALOG INPUT3: MEASURED VOLTAGE
6	ANALOG INPUT2: MEASURED CURRENT
7	ANALOG INPUT1: CURRENT SETPOINT
8	ANALOG OUTPUT1: SETPOINT 1
9	SETPOINT 1 SHIELD
10	SETPOINT 1 RETURN
11	SETPOINT 2 SHIELD
12	INPUT RETURN
13	INPUT RETURN
14	INPUT SHIELD
15	SETPOINT 2 RETURN

Table 6. Pin Assignments For 15-pin D-Sub Analog Connector

The dual output PSI_II can be built as a high speed PSI (fiber optic link operating at 50Mbs) or a low speed PSI (fiber optic link operating at 5Mbs). However, due to board space limitations, the dual output PSI_II cannot be built in Euro-card form.

Table 7 summarizes the different PSI_II configurations.

Configuration	Maximum Speed (Setpoints Per Second)	Number of Outputs	Analog Connector	Assembled in Euro-card
PSI_II	100K	1	9-pin D-sub	Yes
10KHz PSI_II	10K	1	9-pin D-sub	Yes
DUAL OUTPUT PSI_II	100K	2	15-pin D-sub	No
DUAL OUTPUT_10KHZ_PSI_II	10K	2	15-pin D-sub	No

Table 7. PSI_II Configurations

Other Documents And Drawings

A power supply control system consists of a power supply interface unit (PSI) and some form of function generator. The function generator accepts and stores the power supply's ramping function. It also sends each setpoint in the function to the PSI, and save the resultant readbacks.

Since there are various types of function generators and power supply interface units, Table 8 shows the related documents and drawings of these devices.

Modules	User Manual	Schematics
PSC	520_522_Manual.doc	PC-014.pdf
PSI	520_522_Manual.doc	PC-029.pdf
V133	V133_functional_description.doc	BNL drawing: D09-E2980
PSI_II	PSI_II Manual.doc (this document)	BNL drawing: CA3010001
10KHZ PSI_II	PSI_II Manual.doc (this document)	BNL drawing: CA3010001
Dual Output PSI_II	PSI_II Manual.doc (this document)	BNL drawing: CA3010022
10KHZ Dual Output PSI_II	PSI_II Manual.doc (this document)	BNL drawing: CA3010022
V233	V233_functional_description.doc	BNL drawing: CA3010010

Table 8. Documents And Drawings